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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/021,447	10/30/2001	Siuki Chan	X-885 US	6106

24309 7590 07/10/2003

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EXAMINER	
BHAT, ADITYA S	

ART UNIT	PAPER NUMBER
2863	

DATE MAILED: 07/10/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N . 10/021,447	Applicant(s) CHAN, SIUKI	
	Examiner Aditya S Bhat	Art Unit 2863	

-- Th MAILING DATE of this communication appears n the cover sheet with the correspondence address --

Peri d for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 October 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) *10-18* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☒ Claim(s) *5 and 7* is/are objected to.

8)☒ Claim(s) *1-18* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

Combination/subcombination

Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-9, drawn to a method of measuring signal skew of a signal tree, classified in class 702, subclass 125.

II. Claims 10-14, are drawn to a method for programming a programmable device, classified in class 326, subclass 37.

III Claims 15-18, are drawn to a method for calculating a first signal propagation delay, classified in class 333, subclass 141.

The inventions are distinct, each from the other because of the following reasons:

Inventions of each of groups I-III are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, inventions can each be used for their respective uses has separate utility such as dilatometer can be used to measure any gap. See MPEP § 806.05(d).

Because these inventions are distinct for the reasons given above and the search required for Group 1 is not required for Groups 2 and 3, restriction for examination purposes as indicated is proper.

During a telephone conversation with Edel Young on 6/26/03 a provisional election was made ***without traverse*** to prosecute the invention of group !, claims 1-9. Affirmation of this election must be made by applicant in replying to this Office action.

Claims 2-5 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4, 6 and 8-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Honda et al. (USPN 5,497,109)

With regards to claim 1, Honda et al. (USPN 5,497,109) teaches a method of measuring signal skew of a signal tree on a programmable logic device, the device including a signal tree having a source node connected to first, second, and third destination branches, first, second, and third logic blocks programmably connectable to the respective first, second, and third destination branches, each of the logic blocks having an input terminal and an output terminal, the method comprising:

a. instantiating a first delay element on the device using a first programming sequence that includes:
i. connecting the first destination branch to the input terminal of the first logic block; (Col. 1, lines 21-29) and
ii. connecting the output terminal of the first logic block to the input terminal of the second logic block; (Col. 1, lines 21-29) and
b. instantiating a second delay element on the device using a second programming sequence that includes:
i. connecting the third destination branch to the input terminal of the third logic block; (See figure 1) and
ii. connecting the output terminal of the third logic block to the input terminal of the second logic block.(See figure 1)

With regards to claim 2, Honda et al. (USPN 5,497,109) teaches that a signal tree is a clock tree.(Col. 1, lines 21-22)

With regards to claim 3, Honda et al. (USPN 5,497,109) teaches that the input terminal of the second logic block is an asynchronous input terminal. (See figure 8)

With regards to claim 4, Honda et al. (USPN 5,497,109) teaches that the first, second, and third logic blocks are arranged on the device in a column. (See figure 1)

With regards to claim 6, Honda et al. (USPN 5,497,109) teaches that the source node is further connected to fourth, fifth, and sixth destination branches and the programmable logic device further includes fourth, fifth, and sixth logic blocks programmably connectable to the respective fourth, fifth, and sixth destination branches, each of the logic blocks having an input terminal and an output terminal, the method further comprising:

c. instantiating a third delay element on the device using a third programming sequence that includes:

i. connecting the fourth destination branch to the input terminal of the fourth logic block; (See figure 1) and

ii. connecting the output terminal of the fourth logic block to the input terminal of the fifth logic block; (See figure 1) and

d. instantiating a fourth delay element on the device using a fourth programming sequence that includes:

i. connecting the sixth destination branch to the input terminal of the sixth logic block; (See figure 1) and

ii. connecting the output terminal of the sixth logic block to the input terminal of the fifth logic block. (See figure 1)

With regards to claim 8, Honda et al. (USPN 5,497,109) teaches that configuring the device to include the first and second delay elements in respective first and second oscillators. (311; See figure 2)

With regards to claim 9, Honda et al. (USPN 5,497,109) teaches that comparing the periods of the first and second oscillators. (See figure 6)

Claim Objections

Claim 5 is objected to because of the following informalities: Claim 5 recites "The method of claim 4, wherein the second logic block is physically between the first and second logic blocks." A second logic block cannot be between a first and a second logic block. Appropriate correction is required.

Claim 7 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Young (USPN 5,933,023) teaches a FPGA architecture having ram blocks with programmable word length and width and dedicated address and data lines, Choi et al (USPN 6,404,693) teaches a integrated circuit memory devices that select sub-array blocks and input/output line pairs based on input/output bandwidth and methods of controlling the same, Kingsley (USPN 6,144,262) teaches a circuit for measuring signal delays of asynchronous register inputs, Conn Jr. (USPN 6,002,991) teaches a method and apparatus for measuring localized voltages on programmable integrated circuits, Conn Jr. (USPN 5,795,068) teaches a method and apparatus for measuring localized temperatures and voltages on integrated circuits and Jones (USPN 6,507,209) teaches tester accuracy using multiple passes.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aditya S Bhat whose telephone number is 703-308-0332. The examiner can normally be reached on M-F 9-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow can be reached on 703-308-3126. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-5841 for regular communications and 703-308-5841 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Aditya S. Bhat
June 26, 2003

John Barlow
Supervisory Patent Examiner
Technology Center 2800